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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/768,783	01/30/2004	Chang-Hwa Lee	00100.03.0038	7146

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EXAMINER	
CHEN, TSE W	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 08/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/768,783	LEE, CHANG-HWA	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 6, 9 are objected to because of the following informalities:

- As per claim 6, "the step" should be "a step".
- As per claim 9, period after "operation" should be semicolon; "operations" should be "operation".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Zimmer et al, US Publication 20040103272, hereinafter Zimmer.

4. In re claim 1, Zimmer discloses a method for basic input output system loading for a personal computer [fig.2] [0011-12], the method comprising:

- Prior to the availability of system memory, storing data in a cache memory [18] disposed in a central processing unit [10] [0012, 0016, 0021].
- Executing a memory initialization and sizing operation [resource balancing] using the data in the cache memory [0019, 0021, 0023].

5. As per claim 2, Zimmer discloses, wherein the startup operation includes a power on self test operation [bist] [0019].

6. As per claim 3, Zimmer discloses, wherein the cache memory is a level one cache [0012; used a primary memory].

7. As per claim 4, Zimmer discloses, wherein the cache memory is a level two cache [0020; used with main memory].

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zimmer as applied to claim 1 above, and further in view of Lo et al., US Patent 4922451, hereinafter Lo.

10. Zimmer taught each and every limitation of the claim as discussed above. Zimmer did not disclose explicitly that the start-up operation includes a memory sizing operation.

11. Lo discloses a method wherein the start-up operation includes a memory sizing operation [col.4, ll.5-8].

12. It would have been obvious to one of ordinary skill in the art, having the teachings of Lo and Zimmer before him at the time the invention was made, to incorporate the memory sizing operation taught by Lo to the startup operation of Zimmer, as the memory sizing operation is very well known in the art and suitable for use in the startup operation of Zimmer. One of ordinary skill in the art would have been motivated to make such a combination as it provides a

way to determine the actual sizing of memory [Lo: col.4, ll.5-8], necessary for effective functioning of the computer system.

13. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zimmer as applied to claim 1 above, and further in view of Gammel et al., US Publication 20030005314, hereinafter Gammel.

14. Zimmer taught each and every limitation of the claim as discussed above. Zimmer did not discuss the details associated with passing control of the cache memory.

15. Gammel discloses a method wherein a step of passing control of the cache memory includes flushing the cache memory and re-initialize the cache memory [0045; passing of control from initialization to operating system changes programs].

16. It would have been obvious to one of ordinary skill in the art, having the teachings of Gammel and Zimmer before him at the time the invention was made, to modify the teachings of Zimmer to include the teachings of Gammel, in order to obtain the claimed method. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to better secure stored data [Gammel: 0045].

17. Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zimmer as applied to claim 1 above, and further in view of Polyudov, US Publication 20040186988, hereinafter Polyudov.

18. Zimmer taught each and every limitation of the claim as discussed above. Zimmer did not disclose a graphics processor operablely coupled to the central processing unit.

19. In re claim 7, Polyudov discloses a method wherein the start-up operation is performed by a graphics processor [main processor] operablely coupled to the central processing unit [other processors] [0020].

20. It would have been obvious to one of ordinary skill in the art, having the teachings of Polyudov and Zimmer before him at the time the invention was made, to modify the teachings of Zimmer to include the teachings of Polyudov, in order to obtain the claimed method. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to increase processing efficiency by task dividing [Polyudov: 0020].

21. As to claim 8, Polyudov discloses, wherein the graphics processor is disposed within a chipset [0020].

22. Claims 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Polyudov in view of Zimmer.

23. In re claim 9, Polyudov discloses an apparatus [fig.1] for basic input output system loading [0002], the apparatus comprising:

- A graphics processor [54] having a start-up operation [bootable] [0026].
- A central processing unit [other processors of 2] having a memory [associated flash] [0026].
- The graphics processor writing data to the memory prior to the start-up operation [0026; writes to flash prior to starting the processors with updates].

24. Polyudov did not disclose explicitly the central processing unit having a cache memory.

25. Zimmer discloses an apparatus [fig.2] for basic input output system loading [0011-12], the apparatus comprising a central processing unit [10] having a cache memory [14] [fig.1] and writing data to the cache memory prior to the start-up operation [0012, 0016, 0021].

26. It would have been obvious to one of ordinary skill in the art, having the teachings of Polyudov and Zimmer before him at the time the invention was made, to modify the central processing unit taught by Polyudov to include the cache teachings of Zimmer, in order to obtain the central processing unit having a cache memory and associated operations. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to save die space and improve processing capabilities during early initialization [Zimmer: 0005-6, 0021].

27. As per claim 10, Zimmer discloses, wherein the start-up operation performed by the graphics processor includes a power on self test operation [bist] [0019].

28. As per claim 11, Polyudov discloses, wherein the start-up operation performed by the graphics processor includes a memory sizing operation [0033].

29. As per claim 12, Zimmer discloses, wherein the cache memory is a level one cache [0012; used a primary memory].

30. As per claim 13, Zimmer discloses, wherein the cache memory is a level two cache [0020; used with main memory].

31. Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zimmer and Polyudov as applied to claim 9 above, and further in view of Gammel.

32. Zimmer and Polyudov taught each and every limitation of the claim as discussed above. Zimmer and Polyudov disclose, wherein the graphics processor flushes the data from the cache

memory [copies the data to system memory] [Zimmer: 0020]. Zimmer and Polyudov did not disclose reinitializing the cache memory.

33. In re claim 14, Gammel discloses a method comprising re-initialize the cache memory [0045; passing of control from initialization to operating system changes programs].

34. It would have been obvious to one of ordinary skill in the art, having the teachings of Gammel, Polyudov, and Zimmer before him at the time the invention was made, to modify the teachings of Zimmer and Polyudov to include the teachings of Gammel, in order to obtain the claimed method. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to better secure stored data [Gammel: 0045].

35. As to claim 15, Zimmer discloses, wherein the central processing unit thereupon utilizes the cache memory [0020; general purpose use].

36. As to claim 16, Polyudov discloses, wherein the graphics processor is disposed within a chipset [0020].

37. Claims 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zimmer in view of Gammel.

38. In re claim 17, Zimmer discloses a method for basic input output system loading in a graphics processor [10] [fig.2 processes graphics data as is well known in the art] [0011-12], the method comprising:

- Prior to the execution of an operating system, storing data in a cache memory [18] disposed in a central processing unit [10] [0012, 0016, 0021].
- Establishing a stack assignment within the cache memory [0021, 0024].
- Executing a plurality of executable instructions using the cache memory [0019].

- Upon execution of the executable instructions, passing control of the cache memory to the operating system [0011-12, 0019; passing control to finish booting which comprises the operating system as is well known in the art].

39. Zimmer did not discuss the details associated with operations of the cache memory.

40. Gammel discloses a method comprising flushing the cache memory and re-initialize the cache memory [0045; passing of control from initialization to operating system changes programs].

41. It would have been obvious to one of ordinary skill in the art, having the teachings of Gammel and Zimmer before him at the time the invention was made, to modify the teachings of Zimmer to include the teachings of Gammel, in order to obtain the claimed method. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to better secure stored data [Gammel: 0045].

42. As per claim 18, Zimmer discloses, wherein the executable instructions include a power on self test operation [bist] [0019].

43. As per claim 19, Zimmer discloses, wherein the executable instruction are performed by a graphics processing unit [10 processes graphics data as is well known in the art].

44. As per claim 20, Zimmer discloses, wherein the cache memory is a level one cache [0012; used a primary memory].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tse Chen
June 14, 2006

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